UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,853	01/31/2001	Tony San	ALTRP054/A574	3570

22434 7590 12/17/2004

BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY, CA 94704-0778

EXAMINER	
HOGAN, MARY C	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,853	SAN ET AL.	
	Examiner	Art Unit	
	Mary C Hogan	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/31/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. **Claims 1-44** have been examined.

Claim Interpretation

3. **Claims 2 and 17** recite "...substantially the same...": There is no explanation of what "...substantially the same..." means. However, the specification states that "The expected FIR filter response is then compared to the desired FIR filter response and a determination is made whether or not the expected FIR filter response is acceptable or not." **(specification, page 16, lines 8-10)**. From this, it is concluded that "substantially the same" refers to when the design of the filter yields the spectral response that is close to, if not equal, to the desired response.

4. **Claim 44** is directed to "a state machine that controls a select bus coupled to a final multiplexer". There is no explanation of the meaning of this claim in the specification. This claim was interpreted to mean that there is an element in the design of the serial filter that switches between two or more input terminals of the serial filter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-7,11,12,14-22,26,37-40** are rejected under 35 U.S.C. 102(e) as being anticipated by **Dick** et al (U.S. Patent Number 6.600.788), herein referred to as **Dick**.

7. As to **Claims 1 and 16**, **Dick** teaches a filter coefficient generator **(column 3, lines 42-45)**, a filter spectral response simulator **(column 4, lines 8-12)**, a filter resource estimator **(column 7, lines 51-**

57) and a filter compiler unit **(column 5, line 64-column 6, line17)**. As to comparing the desired filter spectral response to the expected filter spectral response, **Dick** teaches implementing the equations that define the transfer function of the filter into a mathematical modeling environment and performing simulations until the design of the filter produces the desired results **(column 7, lines 23-30)**. These simulations involve comparing the desired filter spectral response to the expected filter spectral response.

8. As to **Claims 2 and 17, Dick** teaches performing simulations of the filter until a design that satisfies a specific problem is determined experimentally **(column 7, lines 23-30)**. It is determined that during simulation, filter parameters, such as coefficients, are tweaked until the filter is operating as desired, starting with a set of initial (first set) coefficients. When the simulated spectral response of the filter is substantially the same as what is desired or expected, the coefficients of the simulated model become the coefficients of the filter (or second set) that is to be implemented in the design.

9. As to **Claims 3 and 18, Dick** teaches estimating the implementation cost of the filter **(column 7, lines 51-57)**. Estimating the implementation cost of the filter is done after the design of the filter **(Figure 1, element 13)** is finalized, therefore the second set of filter coefficients would be used.

10. As to **Claims 4 and 19, Dick** teaches a finite impulse response (FIR) filter **(Figure 2)**.

11. As to **Claims 5 and 20, Dick** teaches the filter coefficients are FIR filter coefficients **(Figure 2, elements a_0-a_3)**, wherein the filter spectral response is an FIR filter spectral response **(column 4, lines 8-12)**, wherein the desired filter implementation output file is an FIR filter implementation output file **(column 5, line 64-column 6, line 7)**.

12. As to **Claims 6 and 21, Dick** teaches an FIR filter hardware implementation file provides a routing and placing dataset suitable for fitting the FIR filter in a programmable logic device **(column 5, line 64-column 6, line 17)**, and a filter simulation file **(column 7, lines 23-30)**.

13. As to **Claims 7,11 and 22, Dick** teaches a modulator that re-quantizes input data samples from a high degree of precision to a lower degree of precision thereby reducing the number of resources required to implement the FIR filter in the FPGA **(column 2, lines 26-32)**. It is concluded that a conversion from a floating-point coefficient to a fixed-point coefficient would be a change from a high degree of precision to a low degree of precision. Further, it is concluded that scaling and rounding the floating-point values to form the first set of filter coefficient values would also be a change from a higher degree of precision to a lower degree of precision as taught by **Dick**.

14. As to **Claims 12 and 26, Dick** teaches that the equations that define the transfer function of the filter should be implemented in a mathematical modeling environment such as Matlab **(column 7, lines**

23-28). It is concluded that the Matlab modeling environment would utilize a Matlab Simulink or Testbench model.

15. As to **Claims 14 and 15, Dick** teaches the FIR filter fitted in a programmable integrated circuit such as a programmable logic device **(column 2, lines 20-21)**.

16. As to **Claim 37, Dick** teaches a method of building a decimating filter by a compiler using a plurality of domain polyphases **(column 8, lines 6-11)**, each of the plurality of polyphases is represented by a serial filter **(Figure 6)**, a single clock domain is used for each serial filter, a first clock rule when an input data width is less than or equal to a decimation factor **(column 8, lines 11-14)**, a second clock rule when an input data with is greater than the decimation factor **(column 8, lines 38-41)**.

17. As to **Claim 38, Dick** teaches setting a clock rate to an input data rate, and setting an output data rate equal to the input data rate divided by the decimation factor **(column 7, lines 11-14)**. Further **Dick** teaches that the input sample is processed in a time-multiplexed manner **(column 8, lines 9-11)**, encompassing holding the input data for a number N clock cycles where N is equal to the decimation factor.

18. As to **Claim 39, Dick** teaches setting the clock rate equal to a first speed multiplication factor multiplied by the input data rate **(column 8, lines 38-41)**. It follows from this that the output data rate would then be equal to the multiplication factor times the input data rate divided by the decimation factor as taught **(column 8, lines 11-14)**. Further, **Dick** teaches that the input sample is processed in a time-multiplexed manner **(column 8, lines 9-11)**, encompassing holding the input data for a number L clock cycles where L is equal to the first speed multiplication factor times the decimation factor.

19. As to **Claim 40, Dick** teaches the decimating FIR filter includes a final adder **(column 8, lines 19-21)**.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

22. **Claims 8-10, 23-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dick**, as applied to **Claims 1,16 and 22** above, and further in view of Shung et al (Shung et al, "An Integrated CAD System for Algorithm-Specific IC Design", IEEE Transactions on Computer Aided Design, Vol. 10, No. 4, April 1991), herein referred to as **Shung**.

23. As to **Claim 8-10, 23-25, Dick** teaches implementing equations of the FIR filter design in a mathematical modeling environment and performing simulations until the desired design result is attained **(column 7, lines 23-30)**. Further, **Dick** teaches a modulator that re-quantizes input data samples from a high degree of precision to a lower degree of precision thereby reducing the number of resources required to implement the FIR filter in the FPGA **(column 2, lines 26-32)**. It is concluded that scaling and rounding the floating-point values to form the first set of filter coefficient values would also be a change from a higher degree of precision to a lower degree of precision as taught by **Dick**.

24. **Dick** does not explicitly teach this simulation environment including an input parameter buffer to store a plurality of FIR filter input parameters suitable for implementing the filter, the filter input parameters including a tap quantity value, a pipeline delay value, a parallel FIR filter architecture value, a serial FIR filter architecture value, and input bandwidth value and an initial set of FIR filter component values.

25. **Shung** teaches a CAD system used for the design of a FIR filter **(page 460, section 5.3, first bullet)** including an input parameter buffer to store a plurality of FIR filter input parameters **(page 452, section 4.1, sentence 4)**, wherein the user specifies the target architecture as serial or parallel which encompasses a parallel and serial FIR filter architecture value **(page 448, section 2.2.1, first sentence)**, the data paths which encompass a tap quantity value and pipeline delay value **(page 448, section 2,1,2,**

second paragraph, first sentence), and filter parameters which encompass an input bandwidth value and an initial set of FIR filter coefficient values **(page 448, section 2,1,1, sentences 2 and 3)**.

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the simulation environment as taught in **Shung** as the mathematical modeling environment as disclosed in **Dick** since the environment as taught in **Shung** allows the user to define the target architecture **(page 448, section 2.2.1, first sentence)**, the data paths **(page 448, section 2,1,2, second paragraph, first sentence)**, and filter parameters **(page 448, section 2,1,1, sentences 2 and 3)**.

27. **Claims 13, 27-29, 41-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dick** as applied to **Claims 1,5,16 and 21** above, and further in view of Saramaki et al (Saramaki et al, "Design of Computationally Efficient Interpolated FIR Filters, IEEE Transactions on Circuits and Systems, Vol. 35, No. 1, January 1998), herein referred to as **Saramaki**.

28. As to **Claims 13 and 27-29**, **Dick** teaches a polyphase or multi-rate configuration, such as a decimator **(column 8, lines 6-8)**. Further, **Dick** teaches the FIR filter fitted in a programmable integrated circuit such as a programmable logic device **(column 2, lines 20-21)**.

29. **Dick** does not explicitly teach a multi-rate filter such as an interpolating FIR filter.

30. **Saramaki** teaches interpolating FIR filters and decimation as two approaches to decreasing the required filter length **(page 70, second column, last paragraph)**.

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interpolating FIR filter as taught in **Saramaki** as an alternative to a decimating FIR filter as taught in **Dick** since interpolating FIR filters and decimation filters both reduce the length of filters as taught in **Saramaki (page 70, second column, last paragraph)**.

32. As to **Claim 41**, **Dick** teaches building an FIR filter using a plurality of domain polyphases wherein each of the plurality of polyphases is represented by a serial FIR filter **(column 8, lines 6-8)**.

33. **Dick** does not expressly teach the FIR filter being an interpolating FIR filter and using the interpolation factor for a first and second clock rule.

34. **Saramaki** teaches an interpolating FIR filter as a cascade of FIR filters **(page 70, equation 2 and description)** where the interpolation factor, L, determines how many stages or multipliers a design has **(page 71, paragraph 1)**. Further, **Saramaki** teaches interpolating FIR filters and decimation as two approaches to decreasing the required filter length **(page 70, second column, last paragraph)**.

35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interpolating FIR filter as taught in **Saramaki** as an alternative to a decimating FIR filter as

taught in **Dick** since interpolating FIR filters and decimation filters both reduce the length of filters as taught in **Saramaki (page 70, second column, last paragraph)**. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the interpolation factor, as taught in **Saramaki** to modify the clock rules for a decimation filter as taught in **Dick** since the interpolation factor determines how many stages a design would have as taught in **Saramaki**, making the interpolation factor similar to the decimation factor.

36. As to **Claim 42, Dick** teaches setting a clock rate to an input data rate, and setting an output data rate equal to the input data rate divided by the interpolation factor **(column 7, lines 11-14)** wherein the interpolation factor determines how many stages are included in the filter **(see paragraph 45)**. Further **Dick** teaches that the input sample is processed in a time-multiplexed manner **(column 8, lines 9-11)**, encompassing holding the input data for a number P clock cycles where P is equal to the interpolation factor.

37. As to **Claim 43, Dick** teaches setting the clock rate equal to a second speed multiplication factor multiplied by the input data rate **(column 8, lines 38-41)**. It follows from this that the output data rate would then be equal to the multiplication factor times the input data rate divided by the interpolation factor as taught **(column 8, lines 11-14)** wherein the interpolation factor determines how many stages are included in the filter **(see paragraph 45)**. Further **Dick** teaches that the input sample is processed in a time-multiplexed manner **(column 8, lines 9-11)**, encompassing holding the input data for a number R clock cycles where R is equal to the first speed multiplication factor times the interpolation factor.

38. As to **Claim 44, Dick** teaches the interpolating FIR filter includes a state machine that controls a select bus coupled to a final multiplexer **(Figure 6, element 61)**.

39. **Claims 30-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dick** as applied to **Claims 16 and 21** above, and further in view of Mintzer (Mintzer, Les "Digital Filtering in FPGAs", **Conference Record of the Twenty-Eighth Asilomar Conference on** Signals, Systems and Computers, Vol.2, pages 1373-1377,1994), herein referred to as **Mintzer**.

40. As to **Claims 30, 34 and 36 Dick** teaches estimating the implementation cost of the filter by determining the filter type by showing examples of cost analysis done for different filters **(column 7, line 54 and column 10, line 28)**, a serial filter type **(Figure 6)**, finding a size of a serial tap delay line **(column 7, lines 20-30)**, dividing the second set of filter coefficients into a number N of groups **(column 6, lines 34-44)**, evaluating a number of logic elements required to implement the FIR filter **(column 7,**

line 54), wherein the estimate is a number of logic cells required to implement the FIR filter **(column 7, lines 62-67)**.

41. As to **Claims 31,32,33, and 35, Dick** teaches a parallel filter type **(Figure 8)**, finding size of a parallel tap delay line **(column 7, lines 20-30 and lines 45-48)**, dividing the second set of filter coefficients into a number of groups **(column 6, lines 34-44)**, finding a size of a ROM LUT for a plurality of partial products **(column 7, lines 49-57, Γ(MUL) and lines 62-63)**, and finding a size of an adder tree for the plurality of partial products **(column 7, lines 49-57, Γ(ADD_z^{-1}))**, calculating filter resource estimate wherein the parallel filter resource estimate is a number of logic cells required to implement the parallel filter **(column 7, lines 54, 62-67)**. It is noted that this step would be repeated for additional groups if necessary.

42. **Dick** does not expressly teach determining a filter symmetry.

43. **Mintzer** teaches that exploiting symmetry realizes a significant hardware reduction **(page 1376, column 1, 3rd paragraph)**.

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include filter symmetry as taught in **Mintzer** in the cost estimation as taught in **Dick** since symmetry allows a significant hardware reduction as taught in **Mintzer (page 1376, column 1, 3rd paragraph)**.

Response to Arguments

45. Applicant's arguments filed on 10/21/04 regarding claims 1-44 have been considered but they are not persuasive.

46. As to the argument of the rejection under 35 U.S.C. 112 1st, further examination has determined that the terms used in the specification are known in the art and for this reason, the specification is determined to be enabling. Therefore, the rejection under 35 U.S.C. 112 1st has been removed.

47. Applicant argues: "Dick does not teach or suggest a filter compiler including a filter response estimator", "no resource estimator is coupled to the filter spectral response simulator" and "The material cited by the examiner does not teach or suggest a filter resource estimator and mentions only a resource calculation" (page 13, paragraphs 1 and 2).

48. As to the above arguments, Dick teaches a filter compiler (column 6, lines 3-7), a resource estimator (column 7, lines 33- 67) and a filter spectral response simulator (column 7, lines 23-32) all under the heading of "FPGA Implementation". It is understood to one skilled in the art that after the filter is designed using the simulator, the estimate of the resources, or "real estate" the design will take up on the FPGA will be determined and once the design meets the requirements of the specification in terms of

performance and resources, the design is then compiled for implementation on the FPGA. Therefore, the compiler, simulator, and resource estimator are all "coupled" together in this design process since the output of the design simulator is needed to estimate the resources needed to implement the design and also needed to compile the design. Further, the resource calculation is an estimate of the resources since the design has yet to be implemented.

49. Applicant argues, "Examiner does not indicate where Samaraki teaches or suggests "an input data width" and applying a first or second clock rule...".

50. As to the above argument, it was stated that it would be obvious to modify the clock rules for a decimation filter to use the interpolation factor in place of the decimation factor to develop the clock rules for the interpolation filter since the interpolation factor determines how many stages a design would have as taught in Saramaki, thereby making the interpolation factor similar to the decimation factor (see paragraphs 44 and 45). The "clock rules" mentioned are rules based on the input data with as described in the claims. It is noted that Saramaki does not expressly teach input data width, however, the modification to Dick as stated above encompasses the input data width as mentioned in the claim language since Dick teaches input data width (see paragraph 26).

Conclusion

51. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

52. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 571-272-3712. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C. Hogan
Assistant Patent Examiner
Art Unit 2123

***